Please check that this question paper contains ___9___ questions and ___2___ printed pages within first ten

[Total No. of Questions: 09]
Uni. Roll No.

[Total No. of Pages: 2]

Program: B.Tech. (Batch 2018 onward)
Semester: 3
Name of Subject: Computer Architecture
Subject Code: PCEC-105
Paper ID: 16035
Scientific calculator is Allowed

MORNING
12 MAY 2023

Time Allowed: 03 Hours

Max. Marks: 60

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A

[Marks: 02 each]

1.

a) List the four main components of any general purpose computer.
b) Compare the performance metrics- MIPS, MFLOPS.
c) What is meant by Cache Coherence?
d) Explain the term Multithreading.
e) Analyze the key advantages of SMP over uniprocessor.
f) Compare long term and short term queue.

Part – B

[Marks: 04 each]

2. Discuss Flynn's classification of computers in detail.
3. Explain in detail the motivation behind and organization of Non Uniform Memory Access (NUMA).
4. What are interrupts and their classes? Explain in detail the need for interrupts
5. A benchmark program is run on a 40 MHz processor .The executed program consists of 100,000 instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count	Cycles Per Instruction
Integer Arithmatic	45000	1
Data Transfer	32000	2
Floating Point	15000	2
Control Transfer	8000	2

Determine the effective CPI, MIPS Rate and execution time for this program.

P.T.O.

6. Elaborate using a diagram the steps to add the contents of the memory word at address 940 to the contents of the memory word at address 941 and store the result in the latter location using the fetch and execute cycles.
7. Compare and Contrast the detailed architecture of RISC and CISC.

Part – C **[Marks: 12 each]**

8. Enlist the different elements of Bus Design and explain in detail each of them.

OR

Define Multicore Computers. Explain the hardware performance factors that led to the development of multicore computers and software challenges of exploiting the power of multicore system.

9. Consider the following memory values and a one address machine with accumulator.

Address	Contents
20	40
30	50
40	60
50	70

What values do the following instructions load into the accumulator?

i) LOAD IMMEDIATE 20
ii) LOAD DIRECT 20
iii) LOAD INDIRECT 20
iv) LOAD IMMEDIATE 30
v) LOAD DIRECT 30
vi) LOAD INDIRECT 30

OR

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine.

a. How is a 16 bit memory divided into tag, line number and byte number.
b. Into what lines would bytes with each of the following addresses be stored?
   0001 0001 0001 1011
   1100 0011 0011 0100
   1101 0000 0001 1101
   1010 1010 1010 1010
c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it?
d. How many total bytes of memory can be stored in the cache?
e. Why is the tag also stored in the cache?

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